IN THE CLAIMS:

Please cancel Claims 13-16, without prejudice or disclaimer of the subject matter presented therein.

Please add new Claims 17 and 18 as follows.

Sub E1

17. ~~(New) A memory controller comprising:~~

a converter section adapted to perform serial/parallel conversion of image data of an inputted bit width into image data of ax2n bit width;

a first FIFO (first-in-first-out) section adapted to temporarily store the image data of ax2n bit width;

a frame memory section adapted to store image data of one frame, based on a signal from said first FIFO;

D1 Cont

a second FIFO section adapted to temporarily store image data read out from said frame memory section, and

a control unit adapted to perform a control process, such that image data is read out from said first FIFO section, written into said frame memory section, and read out from said frame memory section at a rate that is half of a rate at which the image data is inputted into said first FIFO section,

wherein said first FIFO section is of a size suitable for storing image data inputted during a period that equals a sum of a period for reading image data from said frame ~~memory unit a plurality of times and a period necessary for command of said frame~~ memory unit.